## CLAIMS

1. A fuse box of a semiconductor device comprising:

a semiconductor substrate having a fuse region;

a lower line placed in the fuse region of the semiconductor substrate, and having a first region and a second region;

an upper line placed on an upper part of the lower line to overlap the first region of the lower line; and

a fuse placed on an upper part of the upper line, and electrically connected to the second region of the lower line and the upper line.

2. The fuse box of a semiconductor device according to claim 1, wherein the fuse is formed of metal line.

3. The fuse box of a semiconductor device according to claim 1, wherein the lower and the upper lines are extended in the same direction toward an outside part of the fuse region from an inside part thereof.

4. The fuse box of a semiconductor device according to claim 1, further comprising:

a lower interlayer insulating layer interposed between the lower and the upper lines; and

an upper interlayer insulating layer interposed between the upper line and the fuse.

5. The fuse box of a semiconductor device according to claim 4, wherein one end of the fuse is electrically connected to the upper line through a first fuse contact hole that penetrates the upper interlayer insulating layer, and the other end of the fuse is electrically connected to the second region of the lower line through a second fuse contact hole that penetrates the upper interlayer insulating layer and the lower interlayer insulating layer.

6. The fuse box of a semiconductor device according to claim 4, further comprising a fuse pad that penetrates a predetermined region of the lower interlayer

insulating layer to contact the second region of the lower line, wherein one end of the fuse is electrically connected to the upper line through a first fuse contact hole that penetrates the upper interlayer insulating layer, and the other end of the fuse is electrically connected to the fuse pad through a second fuse contact hole penetrating the upper interlayer insulating layer.

7. The fuse box of a semiconductor device according to claim 6, further comprising:

a first plate pad formed on an upper surface of the fuse pad;

a second plate pad formed on an upper surface of the upper line, wherein one end of the fuse is electrically connected to the upper line by the second plate pad, and wherein the other end of the fuse is electrically connected to the fuse pad by the first plate pad; and

a plate line separated from the first and second plate pads.

8. The fuse box of a semiconductor device according to claim 6, wherein the fuse pad is separated from the upper line on the lower interlayer insulating layer, but is formed from the same layer as the upper line.

9. The fuse box of a semiconductor device according to claim 7, wherein the first and second plate pads are separated from the plate line in the upper interlayer insulating layer, but are formed of the same layer as the plate line.

10. A semiconductor structure comprising:

a semiconductor substrate having a fuse region;

a first lower line placed on one side of the fuse region that extends toward an outside part of the fuse region, the first lower line having a first region adjacent to a periphery of the fuse region and a second region close to a center of the fuse region;

a second lower line placed on another side of the fuse region that extends toward the outside part of the fuse region, the second lower line having a first region adjacent to the periphery of the fuse region and a second region close to the center of the fuse region, the first lower line and the second lower line symmetrical to each other about a center of the fuse region;

a first upper line placed to overlap the first region of the first lower line;

a second upper line placed to overlap the first region of the second lower line;

a first fuse that is electrically connected to the second region of the first lower line and that is in contact with the upper surface of the first upper line; and

a second fuse that is electrically connected to the second region of the second lower line and that is in contact with the upper surface of the second upper line.

11. The semiconductor structure according to claim 10, wherein the first and the second fuses are formed of metal lines.

12. The fuse box of a semiconductor device according to claim 10, wherein the first lower and the first upper lines extend in a first direction.

13. The semiconductor structure according to claim 12, wherein the second lower and the second upper lines extend in a second direction opposite to the first direction.

14. The semiconductor structure according to claim 10, further comprising:

a lower interlayer insulating layer interposed between the first lower line and the first upper line, and between the second lower line and the second upper line; and

an upper interlayer insulating layer interposed between the first upper line and the first fuse, and between the second upper line and the second fuse.

15. The semiconductor structure according to claim 14, wherein an end of the first and the second fuses is electrically connected to the first and the second upper lines, respectively, through first fuse contact holes penetrating the upper interlayer insulating layer, and wherein another end of the first and the second fuses is electrically connected to the second regions of the first and second lower lines, respectively, through second fuse contact holes penetrating the upper and the lower interlayer insulating layers.

16. The semiconductor structure according to claim 14, further comprising first and second fuse pads penetrating predetermined regions of the lower interlayer insulating layer to contact the second regions of the first and the second lower lines,

respectively, wherein an end of the first and the second fuse is electrically connected to the first and the second upper line, respectively, through first fuse contact holes penetrating the upper interlayer insulating layer, and wherein another end of the first and the second fuse is electrically connected to the first and the second fuse pad, respectively, through second fuse contact holes penetrating the upper interlayer insulating layer.

17. The semiconductor structure according to claim 16, further comprising:

a first plate pad formed on an upper surface of the first upper line, wherein an end of the first fuse is electrically connected to the first upper line by the first plate pad;

a second plate pad formed on an upper surface of the first fuse pad, wherein another end of the first fuse is electrically connected to the first lower line by the second plate pad and the first fuse pad; and

a first plate line separated from the first and second plate pads.

18. The semiconductor structure according to claim 17, further comprising:

a third plate pad formed on an upper surface of the second upper line, wherein an end of the second fuse is electrically connected to the second upper line by the third plate pad;

a fourth plate pad formed on an upper surface of the second fuse pad, wherein another end of the second fuse is electrically connected to the second lower line by the fourth plate pad and the second fuse pad; and

a second plate line separated from the third and fourth plate pads.

19. The semiconductor structure according to claim 16, wherein the first and the second fuse pads are separated from the first and the second upper lines, but are formed from the same layer as the first and the second upper lines.

20. The semiconductor structure according to claim 18, wherein the first, second, third, and fourth plate pads are separated from the first and second plate lines

on the upper interlayer insulating layer, and are formed from the same layer as the first and second plate lines.

21. A method of manufacturing a fuse box of a semiconductor device comprising:

forming a lower line extending toward an inside part of a fuse region on a semiconductor substrate;

forming a lower interlayer insulating layer on a whole surface of the semiconductor substrate having the lower line;

forming an upper line extending toward the inside part of the fuse region on the lower interlayer insulating layer and overlapping the lower line;

forming an upper interlayer insulating layer on a whole surface of the semiconductor substrate having the upper line; and

forming a fuse on the upper interlayer insulating layer that is electrically connected to the lower and the upper lines in the fuse region.

22. The manufacturing method of a fuse box of a semiconductor device according to claim 21, further comprising:

forming a first contact hole in the lower interlayer insulating layer to expose a predetermined portion of the lower line;

forming a fuse pad on the lower interlayer insulating layer that is separated from the upper line and that fills the first contact hole; and

electrically connecting the fuse on the upper interlayer insulating layer to the upper line and the fuse pad.

23. The manufacturing method of a fuse box of a semiconductor device according to claim 22, wherein the predetermined portion is a region adjacent to the center of the fuse region.

24. The manufacturing method of a fuse box of a semiconductor device according to claim 21, wherein the fuse is cut by a laser.

25. A method of manufacturing a semiconductor device comprising:

forming a first group of parallel lower lines on a first side of a fuse region of the semiconductor device, and concurrently, forming a second group of parallel lower lines on a second side of the fuse region, each of the first group of lower lines and a corresponding one of the second group of lower lines extending in opposite directions along a shared axis, and each of the first and the second groups of the lower lines have a first region adjacent to the periphery of the fuse region and a second region closer to the center of the fuse region;

forming a lower interlayer insulating layer on a whole surface of the semiconductor substrate having the first and the second groups of parallel lower lines;

forming a first group of parallel upper lines to overlap the first region of the first group of parallel lower lines and a second group of parallel upper lines to overlap the first region of the second group of parallel lower lines on the lower interlayer insulating layer;

forming an upper interlayer insulating layer on a whole surface of the semiconductor substrate having the first and the second groups of upper lines; and

forming a first group of fuses to overlap the first group of parallel lower lines and a second group of fuses to overlap the second group of parallel lower lines on the upper interlayer insulating layer, both ends of each of the first group of fuses electrically connected to the first group of parallel upper lines and the first group of parallel lower lines located under the first group of fuses, and both ends of each of the second group of fuses electrically connected to the second group of parallel upper lines and the second group of parallel lower lines located under the second group of fuses.

26. The manufacturing method of a semiconductor device according to claim 25, further comprising:

forming first contact holes in the lower interlayer insulating layer to expose predetermined portions of the first and the second groups of parallel lower lines;

forming fuse pads on the lower interlayer insulating layer to be apart from the first and the second groups of parallel upper lines and to fill the first contact holes; and

electrically connecting the first and the second groups of fuses on the upper interlayer insulating layer to the first and the second groups of parallel upper lines, respectively, and to the fuse pads.

27. The manufacturing method of a semiconductor device according to claim 26, wherein the predetermined portions are regions adjacent to the center of the fuse region.

28. The manufacturing method of a semiconductor device according to claim 25, wherein the first and the second groups of the fuses are cut by a laser.